5 Computer Organization

Purpose of This Chapter

• To implement a stored program computer which can execute a set of instructions.

• (A stored program computer behaves as different machines by loading different programs, i.e., sequences of instructions.)
• Computer hardware = registers + ALU + datapath (bus) + control unit.
• The computer goes through **instruction cycles**:
  i) Fetch an instruction from memory;
  ii) Decode the instruction to a sequence of control signals;
  iii) Execute the decoded sequence of microoperations.
• **Control unit**: Instruction → a time sequence of control signals to trigger microoperations.
• Input-output is implemented using an **interrupt cycle**.
5-1. Instruction Codes

– Stored Program Organization: *Fig. 5-1*

  • The simplest way to organize a computer
    – One processor register: AC(Accumulator)
      » The operation is performed with the memory operand and the content of AC

Instruction code format with two parts: Op. Code + Address

  » Op. Code: specify 16 possible operations (4 bit)
  » Address: specify the address of an operand (12 bit)
  » If an operation in an instruction code does not need an operand from memory, the rest of the bits in the instruction (*address field*) can be used for other purpose

– Memory: 12 bit = 4096 word (Instruction and Data are stored)
  » Store each instruction code (*program*) and operand (*data*) in 16-bit memory word

Example
Clear AC, Increment AC, Complement AC, ...
Addressing Mode

• Immediate operand address:
  – the second part of instruction code (address field) specifies the operand

• Direct operand address: **Fig. 5-2(b)**
  – the second part of instruction code specifies the address of the operand

• Indirect operand address: **Fig. 5-2(c)**
  – the bits in the second part of the instruction designate an address of a memory word in which the address of the operand is found (Pointer)

• One bit of the instruction code is used to distinguish between a direct and an indirect address: **Fig. 5-2(a)**

• Effective address: Address where an operand is physically located
Direct Addressing

Occurs When the Operand Part Contains the Address of Needed Data.

1. Address part of IR is placed on the bus and loaded back into the AR

2. Address is selected in memory and its Data placed on the bus to be loaded into the Data Register to be used for requested instructions
Indirect Addressing

Occurs When the Operand Contains the Address of the Address of Needed Data.

1. Address part of IR is placed on the bus and loaded back into the AR

2. Address is selected in memory and placed on the bus to be loaded back into the AR

3. New Address is selected in memory and placed on the bus to be loaded into the DR to use later
Direct and Indirect addressing example
5-2 Computer Registers

- Data Register (DR) : hold the operand (Data) read from memory
  - Accumulator Register (AC) : general purpose processing register
  - Instruction Register (IR) : hold the instruction read from memory
  - Temporary Register (TR) : hold a temporary data during processing
  - Address Register (AR) : hold a memory address, 12 bit width

- Program Counter (PC) :
  - hold the address of the next instruction to be read from memory after the current instruction is executed
  - Instruction words are read and executed in sequence unless a branch instruction is encountered
  - A branch instruction calls for a transfer to a nonconsecutive instruction in the program
  - The address part of a branch instruction is transferred to PC to become the address of the next instruction
  - To read instruction, memory read cycle is initiated, and PC is incremented by one (next instruction fetch)
- **Input Register**(*INPR*) : receive an 8-bit character from an input device

- **Output Register**(*OUTR*) : hold an 8-bit character for an output device

The following registers are used in Mano’s example computer.

<table>
<thead>
<tr>
<th>Register symbol</th>
<th>Number of bits</th>
<th>Register name</th>
<th>Register Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR</td>
<td>16</td>
<td>Data register</td>
<td>Holds memory operands</td>
</tr>
<tr>
<td>AR</td>
<td>12</td>
<td>Address register</td>
<td>Holds address for memory</td>
</tr>
<tr>
<td>AC</td>
<td>16</td>
<td>Accumulator</td>
<td>Processor register</td>
</tr>
<tr>
<td>IR</td>
<td>16</td>
<td>Instruction register</td>
<td>Holds instruction code</td>
</tr>
<tr>
<td>PC</td>
<td>12</td>
<td>Program counter</td>
<td>Holds address of instruction</td>
</tr>
<tr>
<td>TR</td>
<td>16</td>
<td>Temporary register</td>
<td>Holds temporary data</td>
</tr>
<tr>
<td>INPR</td>
<td>8</td>
<td>Input register</td>
<td>Holds input character</td>
</tr>
<tr>
<td>OUTR</td>
<td>8</td>
<td>Output register</td>
<td>Holds output character</td>
</tr>
</tbody>
</table>
Mano’s Computer Figure 5-4

Memory Unit
4096x16

WRITE

READ

AR

LD

INR

CLR

PC

LD

INR

CLR

DR

LD

INR

CLR

AC

LD

INR

CLR

INPR

LD

IR

LD

TR

LD

INR

CLR

OUTR

LD

16-bit common bus

Clock

Address

S₀ S₁ S₂

Bus

Computer System Architecture, Mano, Copyright (C) 1993 Prentice-Hall, Inc.
Common Bus System

- The basic computer has eight registers, a memory unit, and a control unit.

- Paths must be provided to transfer information from one register to another and between memory and registers.

- A more efficient scheme for transferring information in a system with many registers is to use a common bus.

- The connection of the registers and memory of the basic computer to a common bus system: **Fig. 5-4**

  » The outputs of seven registers and memory are connected to the common bus.

  » The specific output is selected by mux(S0, S1, S2):

    - Memory(7), AR(1), PC(2), DR(3), AC(4), IR(5), TR(6)

    - When LD (Load Input) is enable, the particular register receives the data from the bus.

  » Control Input: LD, INC, CLR, Write, Read
COMMON BUS SYSTEM

• **Control variables**: Various control variables are used to select:
  i) the paths of information; &
  ii) the operation of the registers.

➢ **Selection variables**: Used to specify a register whose output is connected to the common bus at any given time.
➢ To select one register out of 8, we need 3 select variables.
➢ For example, if S2S1S0 = 011, the output of DR is directed to the common bus.

➢ **Load input (LD)**: Enables the input of a register connected to the common bus. When LD = 1 for a register, the data on the common bus is read into the register during the next clock pulse transition.

➢ **Increment input (INR)**: Increments the content of a register.

➢ **Clear input (CLR)**: Clear the content of a register to zero.

• When the contents of AR or PC (12 bits) are applied to the 16-bit common bus, the four most significant bits are set to zero. When AR or PC receives information from the bus, only the 12 least significant bits are transferred to the register. Both INPR and OUTR use only the 8 least significant bits of the bus.
Mano’s Computer: Memory Words

- 4-bit opcode Bits 15-12
- How many possible instructions?
  - $2^4 = 16$
- This leaves 12 bits for the address
  - How many words of memory?
  - $2^{12} = 2^2 \cdot 2^{10} = 4K = 4096$ 16-bit words
Mano's Computer: Instructions

- $2^4 = 16$ possible instructions
  - Op-code 0111 reserved for register-reference instructions
  - How many possible register-reference instructions?
  - $2^{12} = 2^2 \cdot 2^{10} = 4K = 4096$ possible r-r instructions (only 12 are used)
Mano's Computer: Instructions

- $2^4 = 16$ possible instructions
  - Op-code 1111 reserved for input/output instructions

- $2^4 = 16$ possible instructions - 0111 (r-r) - 1111 (i/o) = 14 instructions left
  - These are coded as 7 instructions with direct and indirect addressing
5-3. Computer Instruction

- 3 Instruction Code Formats: *Fig. 5-5*

- Memory-reference instruction
  - Opcode = 000 ~ 110
    - \( \text{I=0} : 0xxx \sim 6xxx, \text{I=1} : 8xxx \sim Exxx \)

- Register-reference instruction
  - 7xxx (7800 ~ 7001) : CLA, CMA,

- Input-Output instruction
  - Fxxx (F800 ~ F040) : INP, OUT, ION, SKI,

Reading this table:
the presented code is for any instruction that has 16 bits. The xxx represents don’t care (any data for the first 12 bits). Example 7002 for is a hexadecimal code equivalent to 0111 0000 0000 0010. Which means \( B_1 \) (Bit 1) is set to 1 and the rest of the first 12 bits are set to zeros.
• Instructions are normally stored in consecutive memory locations and are executed sequentially one at a time.
• The **program counter** (PC) holds the address of the next instruction to be read from memory after the current instruction is executed.
• The PC has 12 bits like the AR.
• The instruction read from memory is placed in the **instruction register** (IR) which has 16 bits corresponding to our instruction code length.
• Most processing takes place in the **accumulator** (AC);
• the **temporary register** (TR) is used for holding temporary data during the processing.
• The **input** (INPR) and **output** (OUTR) **registers** hold a character at a time which is read from an input device or to be printed to an output device, respectively. Using the ASCII code, one character is represented with 8 bits (1 byte).
5-4. Timing and Control

- Microprogrammed Control: *Chap. 7*
  - The control information is stored in a control memory, and the control memory is programmed to initiate the required sequence of microoperations
  - Any required change can be done by updating the microprogram in control memory, - Slow operation

- Control Unit: *Fig. 5-6*
  - Control Unit = Control Logic Gate + 3 X 8 Decoder + Instruction Register + Timing Signal
  - Timing Signal = 4 X 16 Decoder + 4-bit Sequence Counter
  - Example) Control timing: *Fig. 5-7*
    - Sequence Counter is cleared when $D_3 T_4 = 1$: $D_3 T_4 : SC \leftarrow 0$
  - Memory R/W cycle time > Clock cycle time
CONTROL UNIT HARDWARE
• Inputs to the control unit come from IR where an instruction read from the memory unit is stored.
• A hardwired control is implemented in the example computer using:
  > A 3´8 decoder to decode opcode bits 12-14 into signals D0, ..., D7;
  > A 4-bit binary sequence counter (SC) to count from 0 to 15 to achieve time sequencing;
  > A 4´16 decoder to decode the output of the counter into 16 timing signals, T0, ..., T15
  > A flip-flop (I) to store the addressing mode bit in IR;
  > A digital circuit with inputs—D0, ..., D7, T0, ..., T15, I, and address bits (11-0) in IR—to generate control outputs supplied to control inputs and select signals of the registers and the bus.
• Clocking principle: The binary counter goes through a cycle, 0000 → 0001 → 0010 → ... → 1111 → 0000. Accordingly only one of T0, ..., T15 is 1 at each clock cycle, T0 → T1 → T2 → ... → T15 → T0; all the other timing signals are 0.
• By setting the clear input (CLR) of SC at a clock cycle, say T3, we can achieve a 4-cycle clock: T0 → T1 → T2 → T3 → T0.
5.5 Instruction Cycle

- A computer goes through the following instruction cycle repeatedly:

  1. Fetch an instruction from memory
  2. Decode the instruction
  3. Read the effective address from memory if the instruction has an indirect address
  4. Execute the instruction until a HALT instruction is encountered

- The fetch & decode phases of the instruction cycle consists of the following microoperations synchronized with the timing signals (clocking principle):

<table>
<thead>
<tr>
<th>Timing signal</th>
<th>Microoperations</th>
</tr>
</thead>
<tbody>
<tr>
<td>T0:</td>
<td>AR ← PC</td>
</tr>
<tr>
<td>T1:</td>
<td>IR ← M[AR], PC ← PC + 1</td>
</tr>
<tr>
<td>T2:</td>
<td>D0, ..., D7 ← Decode IR(12-14), AR ← IR(0-11), I ← IR(15)</td>
</tr>
</tbody>
</table>
0: Since only AR is connected to the address inputs of memory, the address of instruction is transferred from PC to AR.

. Place the content of PC onto the bus by making the bus selection inputs $S2S1S0 = 010$.

. Transfer the content of the bus to AR by enabling the LD input to AR $\text{AR} \leftarrow \text{PC}$.

1: The instruction read from memory is then placed in the instruction register IR. At the same time, PC is incremented to prepare for the address of the next instruction.

. Enable the read input of the memory.

. Place the content of memory onto the bus by making the bus selection inputs $S2S1S0 = 111$. (Note that the address lines are always connected to AR, and we have already placed the next instruction address in AR.)

Transfer the content of the bus to IR by enabling the LD input to IR.
Similar circuits are used to realize the microoperations at T2.

- At T3, microoperations which take place depend on the type of instruction. The four different paths are symbolized as follows, where the control functions must be connected to the proper inputs to activate the desired microoperations.

<table>
<thead>
<tr>
<th>Control function</th>
<th>Microoperation</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7’IT3:</td>
<td>AR ← M[AR], indirect memory transfer</td>
</tr>
<tr>
<td>D7’I’T3:</td>
<td>Nothing, direct memory transfer</td>
</tr>
<tr>
<td>D7I’T3:</td>
<td>Execute a register-reference instruction</td>
</tr>
<tr>
<td>D7IT3:</td>
<td>Execute an I/O</td>
</tr>
</tbody>
</table>

When D7’T3 = 1 (At T3 & IR(12-14) ≠ 111), the execution of memory-reference instructions takes place with the next timing variable T4.
**Figure**: Control circuit for instruction fetch. This is a part of the control circuit and demonstrates the kind of wiring needed.
Figure: Flowchart for fetch & decode phases.
**REGISTER-REFERENCE INSTRUCTIONS**

- The 12 register-reference instructions are recognized by $I = 0$ and $D7 = 1$ ($IR(12-14) = 111$). Each operation is designated by the presence of 1 in one of the bits in $IR(0-11)$. Therefore $D7I'T3 \equiv r = 1$ is common to all register-transfer instructions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Control</th>
<th>Microoperations</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLA</td>
<td>rB_{11}</td>
<td>AC $\leftarrow$ 0</td>
<td>Clear AC</td>
</tr>
<tr>
<td>CLE</td>
<td>rB_{10}</td>
<td>E $\leftarrow$ 0</td>
<td>Clear E</td>
</tr>
<tr>
<td>CMA</td>
<td>rB_{9}</td>
<td>AC $\leftarrow$ AC</td>
<td>Complement AC</td>
</tr>
<tr>
<td>CME</td>
<td>rB_{8}</td>
<td>E $\leftarrow$ E</td>
<td>Complement E</td>
</tr>
<tr>
<td>CIR</td>
<td>rB_{7}</td>
<td>AC $\leftarrow$ shr AC, AC(15) $\leftarrow$ E, E $\leftarrow$ AC(0)</td>
<td>Circular right</td>
</tr>
<tr>
<td>CIL</td>
<td>rB_{6}</td>
<td>AC $\leftarrow$ shl AC, AC(0) $\leftarrow$ E, E $\leftarrow$ AC(15)</td>
<td>Circular left</td>
</tr>
<tr>
<td>INC</td>
<td>rB_{5}</td>
<td>AC $\leftarrow$ AC + 1</td>
<td>Increment AC</td>
</tr>
<tr>
<td>SPA</td>
<td>rB_{4}</td>
<td>If AC(15)=0 then PC $\leftarrow$ PC + 1</td>
<td>Skip if positive</td>
</tr>
<tr>
<td>SNA</td>
<td>rB_{3}</td>
<td>If AC(15)=1 then PC $\leftarrow$ PC + 1</td>
<td>Skip if negative</td>
</tr>
<tr>
<td>SZA</td>
<td>rB_{2}</td>
<td>If AC=0 then PC $\leftarrow$ PC + 1</td>
<td>Skip if AC zero</td>
</tr>
<tr>
<td>SZE</td>
<td>rB_{1}</td>
<td>If E=0 then PC $\leftarrow$ PC + 1</td>
<td>Skip if E zero</td>
</tr>
<tr>
<td>HLT</td>
<td>rB_{0}</td>
<td>S $\leftarrow$ 0 (S is a start-stop flip-flop)</td>
<td>Halt computer</td>
</tr>
</tbody>
</table>
5.6 Memory Reference Instructions

- Opcode (000 - 110) or the decoded output \(D_i\) (\(i = 0, ..., 6\)) are used to select one memory-reference operation out of 7.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Operation decoder</th>
<th>Symbolic description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND</td>
<td>(D_0)</td>
<td>(AC \leftarrow AC \lor M[AR])</td>
</tr>
<tr>
<td>ADD</td>
<td>(D_1)</td>
<td>(AC \leftarrow AC + M[AR], B \leftarrow C_{\text{out}})</td>
</tr>
<tr>
<td>LDA</td>
<td>(D_2)</td>
<td>(AC \leftarrow M[AR])</td>
</tr>
<tr>
<td>STA</td>
<td>(D_3)</td>
<td>(M[AR] \leftarrow AC)</td>
</tr>
<tr>
<td>BUN</td>
<td>(D_4)</td>
<td>(PC \leftarrow AR)</td>
</tr>
<tr>
<td>BSA</td>
<td>(D_5)</td>
<td>(M[AR] \leftarrow PC, PC \leftarrow AR + 1)</td>
</tr>
<tr>
<td>ISZ</td>
<td>(D_6)</td>
<td>(M[AR] \leftarrow M[AR] + 1, \text{If } M[AR] + 1 = 0 \text{ then } PC \leftarrow PC + 1)</td>
</tr>
</tbody>
</table>
5-6. Memory Reference Instruction

- STA : memory write
  \[ D_3T_4 : M[AR] \leftarrow AC, SC \leftarrow 0 \]

- BUN : branch unconditionally
  \[ D_4T_4 : PC \leftarrow AR, SC \leftarrow 0 \]

- BSA : branch and save return address
  \[ D_5T_4 : M[AR] \leftarrow PC, AR \leftarrow AR + 1 \]
  \[ D_5T_5 : PC \leftarrow AR, SC \leftarrow 0 \]
  - Return Address : save return address (135 \leftarrow 21)
  - Subroutine Call : *Fig. 5-10*

- ISZ : increment and skip if zero
  \[ D_6T_4 : DR \leftarrow M[AR] \]
  \[ D_6T_5 : DR \leftarrow DR + 1 \]
  \[ D_6T_6 : M[AR] \leftarrow DR, if(DR = 0) then (PC \leftarrow PC + 1), SC \leftarrow 0 \]

- Control Flowchart : *Fig. 5-11*
  - Flowchart for the 7 memory reference instruction
    - The longest instruction : ISZ(T6)
    - 3 bit Sequence Counter

*Fig. 5-10* Example of BSA

<table>
<thead>
<tr>
<th>PC = 10</th>
<th>BSA 135</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>next instruction</td>
</tr>
<tr>
<td>1</td>
<td>BUN 135</td>
</tr>
<tr>
<td>21</td>
<td>(return address)</td>
</tr>
<tr>
<td>135</td>
<td>Subroutine</td>
</tr>
<tr>
<td>136</td>
<td>PC = 136</td>
</tr>
<tr>
<td>0</td>
<td>M[135] \leftarrow 21(PC), 136(AR) \leftarrow 135 + 1</td>
</tr>
<tr>
<td>1</td>
<td>M[136(PC)] \leftarrow 136(AR), SC \leftarrow 0</td>
</tr>
</tbody>
</table>
Branch and Save Address (BSA)

Subroutine implementation using BSA.
5-7. Input-Output and Interrupt

- 5-7 Input-Output and Interrupt
  - Input-Output Configuration: Fig. 5-12
    - Input Register (INPR), Output Register (OUTR)
      - These two registers communicate with a communication interface serially and with the AC in parallel
      - Each quantity of information has eight bits of an alphanumeric code
    - Input Flag (FGI), Output Flag (FGO)
      - FGI: set when INPR is ready, clear when INPR is empty
      - FGO: set when operation is completed, clear when output device is in the process of printing
  - Input-Output Instruction: Tab. 5-5
    - p = D_7 IT_3
    - IR(i) = B_i \rightarrow IR(6 -11)
    - \textit{\$B_6 - B_{11}$ : 6 I/O Instruction}
  - Program Interrupt
    - I/O Transfer Modes
      - 1) Programmed I/O, 2) Interrupt-initiated I/O, 3) DMA, 4) IOP
      - 2) Interrupt-initiated I/O (FGI FGO 1 Int.)
      - Maskable Interrupt (ION IOF Int. mask)
• Interrupt Cycle: *Fig. 5-13*
  - During the execute phase, IEN is checked by the control
    » IEN = 0: the programmer does not want to use the interrupt, so control continues with the next instruction cycle
    » IEN = 1: the control circuit checks the flag bit, If either flag set to 1, R (R is the interrupt flip flop) is set to 1
  - At the end of the execute phase, control checks the value of R
    » R = 0: instruction cycle
    » R = 1: Interrupt cycle
• Demonstration of the interrupt cycle: *Fig. 5-14*
  - The memory location at address 0 as the place for storing the return address
  - Interrupt Branch to memory location 1
  - Interrupt cycle IEN=0 (*ISR Interrupt ION*)
• The condition for $R = 1$
  \[ T_0T_1T_2'(IEN)(FGI + FGO) : R \leftarrow 1 \]
• Modified Fetch Phase
  - Modified Fetch and Decode Phase
    \[
    \begin{align*}
    RT_0: & AR \leftarrow 0, TR \leftarrow PC \\
    RT_1: & M[AR] \leftarrow TR, PC \leftarrow 0 \\
    RT_2: & PC \leftarrow PC + 1, IEN \leftarrow 0, R \leftarrow 0, SC \leftarrow 0
    \end{align*}
    \]
Fetch and decode instruction

Execute instruction

IEN = 0

FGI = 1

FGO = 0

R = 1

Store return address in location 0

M[0] ← PC

Branch to location 1

PC ← 1

IEN ← 0

R ← 0
### Mano's Computer: RTL

#### TABLE 5-6 Control Functions and Microoperations for the Basic Computer

<table>
<thead>
<tr>
<th>Operation</th>
<th>Microoperation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fetch</strong></td>
<td></td>
</tr>
<tr>
<td>$R.T_0$</td>
<td>$AR ← PC$</td>
</tr>
<tr>
<td>$R.T_1$</td>
<td>$IR ← M[AR]$, $PC ← PC + 1$</td>
</tr>
<tr>
<td>$R.T_2$</td>
<td>$D_0$, ..., $D_{12} ← Decode IR(12-14)$, $AR ← IR(0-11)$, $I ← IR(15)$</td>
</tr>
<tr>
<td><strong>Indirect</strong></td>
<td></td>
</tr>
<tr>
<td>$D.I.T_1$</td>
<td>$AR ← M[AR]$</td>
</tr>
<tr>
<td><strong>Interrupt</strong></td>
<td>$T^2T_0T_1(IEN)(FGI + FGO)$: $R ← 1$</td>
</tr>
<tr>
<td>$RT_0$</td>
<td>$AR ← 0$, $TR ← PC$</td>
</tr>
<tr>
<td>$RT_1$</td>
<td>$M[AR] ← TR$, $PC ← 0$</td>
</tr>
<tr>
<td>$RT_2$</td>
<td>$PC ← PC + 1$, $IEN ← 0$, $R ← 0$, $SC ← 0$</td>
</tr>
<tr>
<td><strong>Memory-reference</strong></td>
<td></td>
</tr>
<tr>
<td>AND</td>
<td>$D.T_0$</td>
</tr>
<tr>
<td>$D.T_0$</td>
<td>$DR ← M[AR]$</td>
</tr>
<tr>
<td>$D.T_1$</td>
<td>$AC ← AC ∧ DR$, $SC ← 0$</td>
</tr>
<tr>
<td>ADD</td>
<td>$D.T_0$</td>
</tr>
<tr>
<td>$D.T_0$</td>
<td>$DR ← M[AR]$</td>
</tr>
<tr>
<td>$D.T_1$</td>
<td>$AC ← AC + DR$, $E ← C_{out}$, $SC ← 0$</td>
</tr>
<tr>
<td>LDA</td>
<td>$D.T_0$</td>
</tr>
<tr>
<td>$D.T_0$</td>
<td>$DR ← M[AR]$</td>
</tr>
<tr>
<td>$D.T_1$</td>
<td>$AC ← DR$, $SC ← 0$</td>
</tr>
<tr>
<td>STA</td>
<td>$D.T_0$</td>
</tr>
<tr>
<td>$D.T_0$</td>
<td>$M[AR] ← AC$, $SC ← 0$</td>
</tr>
<tr>
<td>BUN</td>
<td>$D.T_0$</td>
</tr>
<tr>
<td>$D.T_0$</td>
<td>$PC ← AR$, $SC ← 0$</td>
</tr>
<tr>
<td>BSA</td>
<td>$D.T_0$</td>
</tr>
<tr>
<td>$D.T_0$</td>
<td>$M[AR] ← PC$, $AR ← AR + 1$</td>
</tr>
<tr>
<td>$D.T_1$</td>
<td>$PC ← AR$, $SC ← 0$</td>
</tr>
<tr>
<td>ISZ</td>
<td>$D.T_0$</td>
</tr>
<tr>
<td>$D.T_0$</td>
<td>$DR ← M[AR]$</td>
</tr>
<tr>
<td>$D.T_1$</td>
<td>$DR ← DR + 1$</td>
</tr>
<tr>
<td>$D.T_2$</td>
<td>$M[AR] ← DR$, if $(DR = 0)$ then $(PC ← PC + 1)$, $SC ← 0$</td>
</tr>
<tr>
<td><strong>Register-reference</strong></td>
<td></td>
</tr>
<tr>
<td>$D.T_0.T_1 = r$</td>
<td>(common to all register-reference instructions)</td>
</tr>
<tr>
<td><strong>Input-output</strong></td>
<td></td>
</tr>
<tr>
<td>$IR(i) = B_i$ $(i = 0, 1, 2, ..., 11)$</td>
<td></td>
</tr>
<tr>
<td>$r$:</td>
<td>$SC ← 0$</td>
</tr>
<tr>
<td>CLA</td>
<td>$r.B_{11}$</td>
</tr>
<tr>
<td>$r.B_{11}$</td>
<td>$AC ← 0$</td>
</tr>
<tr>
<td>CLE</td>
<td>$r.B_{10}$</td>
</tr>
<tr>
<td>$r.B_{10}$</td>
<td>$E ← 0$</td>
</tr>
<tr>
<td>CMA</td>
<td>$r.B_9$</td>
</tr>
<tr>
<td>$r.B_9$</td>
<td>$AC ← AC$</td>
</tr>
<tr>
<td>CME</td>
<td>$r.B_8$</td>
</tr>
<tr>
<td>$r.B_8$</td>
<td>$E ← E$</td>
</tr>
<tr>
<td>CIR</td>
<td>$r.B_7$</td>
</tr>
<tr>
<td>$r.B_7$</td>
<td>$AC ← shr AC$, $AC(15) ← E$, $E ← AC(0)$</td>
</tr>
<tr>
<td>INC</td>
<td>$r.B_6$</td>
</tr>
<tr>
<td>$r.B_6$</td>
<td>$AC ← AC + 1$</td>
</tr>
<tr>
<td>SPA</td>
<td>$r.B_5$</td>
</tr>
<tr>
<td>$r.B_5$</td>
<td>$If (AC(15) = 0)$ then $(PC ← PC + 1)$</td>
</tr>
<tr>
<td>SNA</td>
<td>$r.B_4$</td>
</tr>
<tr>
<td>$r.B_4$</td>
<td>$If (AC(15) = 1)$ then $(PC ← PC + 1)$</td>
</tr>
<tr>
<td>SZA</td>
<td>$r.B_3$</td>
</tr>
<tr>
<td>$r.B_3$</td>
<td>$If (AC = 0)$ then $(PC ← PC + 1)$</td>
</tr>
<tr>
<td>SZE</td>
<td>$r.B_2$</td>
</tr>
<tr>
<td>$r.B_2$</td>
<td>$If (E = 0)$ then $(PC ← PC + 1)$</td>
</tr>
<tr>
<td>HLT</td>
<td>$r.B_1$</td>
</tr>
<tr>
<td>$r.B_1$</td>
<td>$S ← 0$</td>
</tr>
<tr>
<td>INP</td>
<td>$p.B_{11}$</td>
</tr>
<tr>
<td>$p.B_{11}$</td>
<td>$AC(0-7) ← INPR$, $FGI ← 0$</td>
</tr>
<tr>
<td>OUT</td>
<td>$p.B_9$</td>
</tr>
<tr>
<td>$p.B_9$</td>
<td>$OUTR ← AC(0-7)$, $FGO ← 0$</td>
</tr>
<tr>
<td>SKE</td>
<td>$p.B_8$</td>
</tr>
<tr>
<td>$p.B_8$</td>
<td>$If (FGI = 1)$ then $(PC ← PC + 1)$</td>
</tr>
<tr>
<td>SKO</td>
<td>$p.B_7$</td>
</tr>
<tr>
<td>$p.B_7$</td>
<td>$If (FGO = 1)$ then $(PC ← PC + 1)$</td>
</tr>
<tr>
<td>ION</td>
<td>$p.B_6$</td>
</tr>
<tr>
<td>$p.B_6$</td>
<td>$IEN ← 1$</td>
</tr>
<tr>
<td>IOF</td>
<td>$p.B_5$</td>
</tr>
<tr>
<td>$p.B_5$</td>
<td>$IEN ← 0$</td>
</tr>
</tbody>
</table>
5-8. Complete Computer Description

- 5-8 Complete Computer Description
  - The final flowchart of the instruction cycle: Fig. 5-15
  - The control function and microoperation: Table. 5-6
- 5-9 Design of Basic Computer
  - The basic computer consists of the following hardware components
    - 1. A memory unit with 4096 words of 16 bits
    - 2. Nine registers: AR, PC, DR, AC, IR, TR, OUTR, INPR, and SC (Fig. 2-11)
    - 3. Seven F/Fs: I, S, E, R, IEN, FGI, and FGO
    - 4. Two decoders in control unit: 3 x 8 operation decoder, 4 x 16 timing decoder (Fig. 5-6)
    - 5. A 16-bit common bus (Fig. 5-4)
    - 6. Control Logic Gates: Fig. 5-6
    - 7. Adder and Logic circuit connected to the AC input
      - Control Logic Gates
        - 1. Signals to control the inputs of the nine registers
        - 2. Signals to control the read and write inputs of memory
        - 3. Signals to set, clear, or complement the F/Fs
        - 4. Signals for $S_2 S_1 S_0$ to select a register for the bus
        - 5. Signals to control the AC adder and logic circuit
Since memory is 4K in size, it requires 12 address bits. Each word of memory contains 16 bits of data. Similarly, the program counter (PC) is also 12 bits wide. Each data word is 16 bits wide. The Data Register (DR) must also be 16 bits wide, since it receives data from and sends data to memory. The accumulator (AC) acts on 16 bits of data. The Instruction Register (IR) receives instruction codes from memory which are 16 bits wide.

TR is a temporary register. Only the CPU can cause it to be accessed. The programmer cannot directly manipulate the contents of TR. Most CPU’s have one or more temporary registers which it uses to perform instructions. The input and output registers (INPR and OUTR) are 8 bits wide each. For this CPU, I/O instructions only transfer 8 bits of data at a time. The 3-bit sequence counter (SC) is used to generate the correct timing (T) states. Other 1-bit registers are the carry out (E), the indirect register (I), the interrupt enable (IEN) and the input and output flags (FGI and FGO).
• The control unit must make sure that at most one register (or memory unit) places data onto the bus at one time.

• The memory unit is external to the CPU. It always receives its address from the address register (AR) and makes its data available to the CPU bus. It receives data from the CPU bus as well.

• Read and write signals are supplied by the control unit.

• The address registers, program counter (PC) and data register (DR) each load data onto and receive data from the system bus. Each has a load, increment and clear signal derived from the control unit. These signals are synchronous; each register combines these signals with the system clock to activate the proper function.

• Since AR and PC are only 12-bits each, they use the low order 12 bits of the bus.
• The accumulator makes its data available on the bus but does not receive data from the bus.

• It receives data from ALU (Adder and Logic) only.

• To load data into AC, place it onto the bus via DR and pass it directly through the ALU.

• Note that E, the 1-bit carry flag, also receives its data from the ALU.

• The input register, INPR, receives data from an external input port and makes it available only to AC.

• The output register makes its data available to the output port using specific hardware.

• The instruction register, IR, can only be loaded; it cannot be incremented nor cleared. Its output is used to generate D_i’s and T_i’s control signals.

• TR is a temporary register. The CPU uses this register to store intermediate results of operations. It is not accessible by the external programs. It is loaded, incremented and cleared like the other registers.
Register reference instructions are those which access data and manipulate the contents of registers.

- They do not access memory.
- These instructions are executed in one clock cycle.

Each register reference instruction is performed in a single clock cycle.
Each instruction manipulates the contents of a register within the CPU, so the relatively time consuming accesses to memory are avoided.

There are 12 register reference instructions overall, each of which is encoded by one of the 12 low order bits of the instruction code.
This class of instructions accesses I/O devices.

The instructions in this class also enable and disable interrupts. Since this computer only allows for a single input device and a single output device, no address information is needed.

The input/output instructions are performed in a single clock cycle.

Note that there are no instructions to set FGI or FGO to 1.

These flags are set by external hardware when input data is ready or output data is requested. When the CPU performs the proper input or output instruction (INP or OUT), it resets the flag to allow for future I/O data transfers.
Control signals

- T0, T1, ... T6 : Timing signals
- D0, D1, ... D7 : Decoded instruction
- I: Indirect bit
- R: Interrupt cycle bit

- The T signals occur in sequence and are never skipped over. The only two options during a T-state are to proceed to the next T-state or to return to T state 0.

- The D signals decode the instruction and are used to select the correct execute routine.

- I is used to select the indirect routine and also to select the correct execute routine for non-memory reference instructions.

- R is used for interrupt processing and will be explained later.
Control signals

This circuit generates the T signals. The sequence counter, SC, is incremented once per clock cycle. Its outputs are fed into a 3-8 decoder which generates the T signals. Whenever a micro-operation sets SC to zero, it resets the counter, causing T0 to be activated during the next clock cycle.
The D signals are generated in a similar way as the T signals. For the D signals, the source is IR(14-12) instead of SC. Also note that IR won’t change during the instruction execution.
In this example, the instruction AND I 500 is fetched from memory location 100.

• During T0, the address (100) is loaded into AR.

• During T1, the instruction code is loaded into IR and PC is incremented.

• In T2, the address portion of this instruction, 500, is loaded into AR. The indirect register gets 1, the value of the indirect bit of the instruction. Since bits 14-12 are 000, D0 is activated by the decoder. These tell us that we have an indirect AND instruction.

• In T3, D7 is ‘0’ and I is ‘1’, the address portion of the instruction is not the address of the operand. It is the address of a memory location which contains address of actual operand. Look in memory to get the actual address, 234, which is loaded into AR.
AND execute cycle

AND:

D0T4: DR ← M[AR]

D0T5: AC ← AC ^ DR, SC ← 0

Example: AND 500: AC = 31, M[500] = 25

D0T4: DR ← 25

D0T5: AC ← 31 ^ 25 = 21, SC ← 0

In this and all examples, all data is given in hex. Here, the instruction cycle has fetched the AND instruction, determined that this execute routine must perform and load address 500 into the AR.

• In T4, the data is read from memory and loaded into the DR, 25 in this case. Next,
• in T5, it is logically ANDed with the current contents of the accumulator, 31 here, and the result is stored back into the accumulator. Setting SC to zero returns to the fetch routine to access the next instruction.
The ADD operation proceeds similarly to the AND operation. The only difference is that once the operand is loaded from memory it is arithmetically added to the current contents of the accumulator.
LDA execute cycle

LDA:

D2T4: DR ← M[AR]

D2T5: AC ← DR, SC ← 0

Example: LDA 500: M[500] = 25

D2T4: DR ← 25

D2T5: AC ← 25, SC ← 0

As in the previous instructions, the CPU reads the data from memory into DR during T4. In the following cycle, this data is copied into the accumulator.

Since the accumulator only receives data from the adder and logic section, the data from DR is passed into this unit and then passed through it unchanged.
The STA instruction is much more straightforward than the LDA instruction.

Since the address is already available from AR to the memory unit, we simply move data directly from the accumulator to the memory unit in a single clock cycle.
The BUN instruction implements a jump by loading the new address directly from AR into the PC. Unlike many of the other memory reference instructions, BUN receives its data as part of the original instruction and does not require a secondary memory access.
The BSA instruction implements a subroutine call.

• A BSA for address X stores the return address at location X.

• Note that PC was incremented as part of the opcode fetch and thus contains the return address. AR contains X.

• During T4, AR is incremented to X+1, since this is the start of the actual subroutine code.

• T5 loads the value X+1 into the program counter and returns to the fetch routine. Note that this computer cannot implement recursion. If a subroutine called itself, it would overwrite the original return address and would be caught in the subroutine forever! We return from a subroutine by using a BUN I X instruction.
Subroutine call using BSA

Example: 100: BSA 200

D5T4: M[AR] ← PC, AR ← AR+1

M[200] ← 101, AR ← 201

D5T5: PC ← AR, SC ← 0

PC ← 201, SC ← 0

• During T4, the return address, 101, is loaded into memory location 200 and AR is set to 201. This value is the location of the first instruction of the subroutine.

• During T5 it is loaded into the program counter.

• The computer will next fetch the instruction at this location.
Subroutine return using BUN I

Example: 205: BUN I 200

M[200] = 101

D7I’T3: AR ← M[AR](11-0)

AR ← M[200](11-0) = 101

D4T4: PC ← AR, SC ← 0

PC ← 101, SC ← 0

• In this example we perform a return from a previous subroutine.

• After executing a few instructions which comprise the subroutine, we reach the BUN I 200 instruction.

• During the indirect cycle, we go to location 200 to get the actual address we want, in this case 101.

• During T4, we load this value into the program counter, affecting the jump.
The ISZ instruction is used for program loops. The negative of the count value is stored in some memory location, say X. At the end of the loop, we place the instruction ISZ X. During T4, the Basic Computer copies the contents of memory location X into the data register. This value is incremented during T5, and written back into memory during T6. (AR still contains the memory address at this point.) Also during T6, this value, still available in DR, is check to see if it is zero. If so, PC is incremented, in effect skipping the next instruction.
Loop control using ISZ

Example: 100: ISZ 200 M[200] = 55

D6T4: DR ← M[AR] (DR ← 55)
D6T5: DR ← DR+1 (DR ← 56)
D6T6: M[AR] ← DR, SC ← 0,
if (DR=0) then PC ← PC+1
(M[200] ← 56, SC ← 0)

In this example, memory location 200 contains 55, which is loaded into the data register during T4. It is incremented to 56 during T5 and stored back into memory location 200. Since it is not zero, we do not increment the PC.
Loops using ISZ

X: Start of loop

ISZ 200
BUN X

Continue on...

Here is an example of how to use the ISZ instruction in a program loop. The loop starts at some location X and does its work. Then we perform the ISZ instruction, which increments the loop counter. If it is not zero, it does not skip the next instruction. It executes that instruction, which branches back to the beginning of the loop. If it is zero, it skips the BUN X instruction, exiting the loop.
There are 12 register reference instructions, each activated by one of the 12 low order bits of the instruction register. Each register reference instruction is executed in a single clock cycle.

- \( r: \text{SC} \leftarrow 0 \). This means that \( \text{SC} \leftarrow 0 \) whenever \( r=1 \), regardless of the values of IR(11-0). In short, this is equivalent to adding the micro-operation \( \text{SC} \leftarrow 0 \) to each of these instructions individually. The CLA and CLE instructions clear AC and E. CMA and CME perform complement. CIR and CIL perform circular right and left shifts.
Register-reference execute cycles

\[ r = D7I'T3 \]
\[ r: SC \leftarrow 0 \]

\textbf{(INC)} \( rIR5: \) \( EAC \leftarrow AC+1 \)

\textbf{(SPA)} \( rIR4: \) IF \( AC(15)=0 \) THEN \( PC \leftarrow PC+1 \)

\textbf{(SNA)} \( rIR3: \) IF \( AC(15)=1 \) THEN \( PC \leftarrow PC+1 \)

\textbf{(SZA)} \( rIR2: \) IF \( AC=0 \) THEN \( PC \leftarrow PC+1 \)

\textbf{(SZE)} \( rIR1: \) IF \( E=0 \) THEN \( PC \leftarrow PC+1 \)

\textbf{(HLT)} \( rIR0: \) \textbf{HALT}

The INC instruction increments AC, storing the result in register pair E/AC. The next four instructions skip an instruction in the program if AC is positive (SPA), AC is negative (SNA), AC is zero (SZA) or E is zero (SZE). Note that SPA actually skips an instruction if AC is not negative, since it also skips an instruction if AC is zero. The HLT instruction shuts down the computer.
The Basic Computer has one 8-bit input port and one 8-bit output port. Each port interface is modeled as an 8-bit register which can send data to or receive data from AC(7-0). Whenever input data is to be made available, the external input port writes the data to INPR and sets FGI to 1. When the output port requests data, it sets FGO to 1. As will be shown shortly, the FGI and FGO flags are used to trigger interrupts (if interrupts are enabled by the IEN flag).
I/O execute cycles

\[ p = D7IT3 \quad p: \ SC \leftarrow 0 \]

(INP) \( pIR11: \ AC(7-0) \leftarrow \ INPR, \ FGI \leftarrow 0 \)

(OUT) \( pIR10: \ OUTR \leftarrow \ AC(7-0), \ FG0 \leftarrow 0 \)

(SKI) \( pIR9: \ IF \ FGI = 1 \ THEN \ PC \leftarrow \ PC+1 \)

(SKO) \( pIR8: \ IF \ FGO = 1 \ THEN \ PC \leftarrow \ PC+1 \)

(ION) \( pIR7: \ IEN \leftarrow 1 \)

(IOF) \( pIR6: \ IEN \leftarrow 0 \)

Once data is made available to the CPU, it can be read in using the INP instruction. Note that this not only reads the data into the accumulator, but also resets FGI to zero. This tells the input port that it may send more data. In a similar manner, the OUT instruction writes data to OUTR and resets FGO to zero, notifying the output port that data is available. The SKI and SKO instructions skip an instruction if there is a pending input or output request. This is useful in determining the I/O request which caused an interrupt to occur. ION and IOF enable and disable interrupts. Interrupts will be explained more fully shortly.
Input operation

- Input device makes data available and sets FGI=1.
- If interrupt is enabled, Basic Computer calls interrupt routine at location 0, which disables further interrupts.
- Interrupt routine reads in and processes data, re-enables interrupts and returns. Reading in data resets FGI to zero.

In the Basic Computer, I/O requests are processed as interrupts. This process is followed for input requests. The input will only be processed if interrupts are enabled. It will be ignored, but will remain pending, if interrupts are disabled.
Output operation

- Output device requests data and sets FGO=1.
- *If interrupt is enabled*, Basic Computer calls interrupt routine at location 0, which disables further interrupts.
- Interrupt routine processes and outputs data, re-enables interrupts and returns. Writing out data resets FGO to zero.

Outputs are handled similarly to inputs. Note that both input and output interrupts call an interrupt service routine at location 0. There is only one routine for both input and output, so it must distinguish between the two. This is where the SKI and SKO instructions become useful.
Interrupt processing

An interrupt occurs if the interrupt is enabled (IEN = 1) AND an interrupt is pending (FG1 or FGO = 1).

Before processing the interrupt, *complete the current instruction*!!!

Call the interrupt service routine at address 0 and disable interrupts.

It is of the utmost importance to complete the current instruction, otherwise the CPU will not perform properly.

The interrupt service routine is called by the CPU in a manner similar to the execution of the BSA instruction.
An interrupt is asserted by setting R to 1. This occurs when interrupts are enabled (IEN) and there is either an input or output request (FGI+FGO). We must also have completed the current fetch cycle (T0’T1’T2’).

When we look at the code to implement the interrupt cycle, we see why we must wait until after T2 to set R to 1. If we set R to 1 during T0, for example, the next micro-instruction would be RT1, right in the middle of the interrupt cycle. Since we want to either perform an entire opcode fetch or an entire interrupt cycle, we don’t set R until after T2.
The interrupt cycle acts like a BSA 0 instruction.

• During T0 we write a 0 into AR and copy the contents of PC, the return address, to TR.

• We then store the return address to location 0 and clear the program counter during T1.

• In T2, we increment PC to 1, clear the interrupt enable, set R to zero (because we’ve finished the interrupt cycle) and clear SC to bring us back to T0.

Note that IEN is set to 0. This disables further interrupts. If another interrupt occurred while one was being serviced, the second interrupt would write its return address into location 0, overwriting the interrupt return address of the original routine. Then it would not be possible to return to the program properly.
Modified fetch cycle

R’T0: AR ← PC

R’T1: IR ← M[AR], PC ← PC+1

R’T2: AR ← IR(11-0), I ← IR15,

D0, D1, ... D7 ← Decode IR(14-12)

This is exactly the same as before, but R’ insures that no interrupts must be serviced.
5-9 Design of Basic Computer

- Two basic things are needed: data paths and control signals
- A hardwired-control implementation: Stitch together the individual pieces of the data path.
- The microoperation table provides sufficient information to implement the circuits for control (wiring various gates).

**Figure**: Where the control resides in the computer.
Input:
1. D0 - D7: Decoded IR(14-12)
2. T0 - T15 : Timing signals
3. I: Indirect signal
4. IR(0-11)

Output:
1. Control inputs of the nine registers, AR, PC, DR, AC, IR, TR, OUTR, INPR, SC
2. Read and write inputs of memory
3. Signals to set, clear, or complement the flip-flops, IEN, R, etc.
4. Select signals, S2, S1, S0, for common bus
5. Control signals to the AC adder and logic circuit

CONTROL OF REGISTERS AND MEMORY

Systematic Design Procedure
1. For a given register, scan the table of microoperations in the previous slides to find all the statements involving that gate.
2. Translate the associated control functions to Boolean functions.
3. Convert the Boolean expressions into logic gates.
Example: Control of AR
1. The following is the summary of the register transfers associated with the address register.
   
   \[
   \begin{align*}
   &R'T0: \ AR \leftarrow PC \ load \\
   &R'T2: \ AR \leftarrow IR(0-11) \ load \\
   &D7'IT3: \ AR \leftarrow M[AR] \ load \\
   &RT0: \ AR \leftarrow 0 \ clear \\
   &D5T4: \ AR \leftarrow AR + 1 \ increment
   \end{align*}
   \]

2. The control functions can be combined into the following Boolean expressions.
   
   \[
   \begin{align*}
   &LD(AR) = R'T0 + R'T2 + D7'IT3 \\
   &CLR(AR) = RT0 \\
   &INR(AR) = D5T4
   \end{align*}
   \]
3. The previous Boolean expressions can be converted to the following logic gates.

- In a similar fashion, the control gates for the other registers and memory can be derived. For example, the logic gates associated with the read input of memory is derived by scanning the microoperation table to find the statements that specify a read operation. The read operation is recognized from the symbol $\leftarrow M[AR]$. 

$$\text{Read} = R'T1 + D7'I'T3 + (D0 + D1 + D2 + D3)T4$$
5-9 Design of Basic Computer

- Register Control: AR
  - Control inputs of AR: LD, INR, CLR
  - **Find all the statements that change the AR in Table. 5-6**
  - Control functions
    
    \[
    \begin{align*}
    LD(AR) &= R'T_0 + R'T_1 + D_7'I'T_3 \\
    CLR(AR) &= RT_0 \\
    INR(AR) &= D_5'T_4
    \end{align*}
    \]

- Memory Control: READ
  - Control inputs of Memory: READ, WRITE
  - Find all the statements that specify a read operation in Table. 5-6
  - Control function
    
    \[
    \text{READ} = R'T_1 + D_7'I'T_3 + (D_0 + D_1 + D_2 + D_3)T_4
    \]

- F/F Control: IEN
  - Control functions
    
    \[
    \begin{align*}
    pB_7 : IEN &\leftarrow 1 \\
    pB_6 : IEN &\leftarrow 0 \\
    RT_2 : IEN &\leftarrow 0
    \end{align*}
    \]
5-9. Design of Basic Computer

- Bus Control
  
  • Encoder for Bus Selection: *Table. 5-7*
    
    \[ S_0 = x_1 + x_3 + x_5 + x_7 \]
    \[ S_1 = x_2 + x_3 + x_6 + x_7 \]
    \[ S_0 = x_4 + x_5 + x_5 + x_7 \]
  
  • \( x_1 = 1 \):
    
    \[ \text{Bus} \leftarrow \text{AR} = \text{Find} ? \leftarrow \text{AR} \]
    
    \[ D_4T_4 : \text{PC} \leftarrow \text{AR} \]
    \[ D_5T_5 : \text{PC} \leftarrow \text{AR} \]
  
  - Control Function:
    
    \[ x_1 = D_4T_4 + D_5T_5 \]
    
  • \( x_2 = 1 \):
    
    \[ \text{Bus} \leftarrow \text{PC} = \text{Find} ? \leftarrow \text{PC} \]
    
    \[ \text{Bus} \leftarrow \text{Memory} = \text{Find} ? \leftarrow M[\text{AR}] \]
  
  • \( x_7 = 1 \):
    
    \[ x_7 = R'T_1 + D_7'IT_3 + (D_0 + D_1 + D_2 + D_3)T_4 \]
    
    - Same as Memory Read
    - Control Function:

\[ x_1 = 1 \] corresponds to the bus connection of AR as a source.
5-10. Design of Accumulator Logic

- 5-10 Design of Accumulator Logic
  - Circuits associated with AC: *Fig. 5-19*
5-10. Design of Accumulator Logic

Control of AC: *Fig. 5-20*

- Find the statement that change the AC: $AC \leftarrow ?$

\[\begin{align*}
D_0T_5 & : AC \leftarrow AC \land DR \\
D_1T_5 & : AC \leftarrow AC + DR \\
D_2T_5 & : AC \leftarrow DR \\
pB_{11} & : AC(0-7) \leftarrow \text{INPR} \\
rB_9 & : AC \leftarrow \overline{AC} \\
rB_7 & : AC \leftarrow \text{shr } AC, AC(15) \leftarrow E \\
rB_6 & : AC \leftarrow \text{shr } AC, AC(0) \leftarrow E \\
rB_{11} & : AC \leftarrow 0 \\
rB_5 & : AC \leftarrow AC + 1
\end{align*}\]
5-10. Design of Accumulator Logic

- Adder and Logic Circuit: *Fig. 5-21 (16 bit)*
Summary of Mano’s Computer

- Fig. 5-4 : Common Bus (p.130)
- Fig. 2-11 : Register (p. 59)
- Fig. 5-6 : Control Unit (p. 137)
- Fig. 5-16, 17,18 : Control Logic Gates (p.161-163)
  - Fig. 5-4 Component Control Input
  - Register, Memory, F/Fs, Bus Selection
- Fig. 5-20 : AC control (p.165)
- Fig. 5-21 : Adder and Logic (p.166)